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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,495	10/13/2000	Sean Timothy Crowley	45475-0001999-58164	9398

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EXAMINER
GEYER, SCOTT B

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/687,495	Applicant(s) CROWLEY ET AL.
	Examiner Scott B. Geyer	Art Unit 2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,13,14,17-23 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,13,14,17-23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *17 September 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 9-17-02. These drawings are acceptable. Formal drawings reflecting the changes made are required in response to this action.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 4, 6, 7, 13, 14, 17-23 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Glenn (6,143,981).

As to **independent claim 1**, Glenn teaches a semiconductor chip with a plurality of input/output pads (figure 8, numeral 56a), a chip paddle (24) which is adjacent a bottom surface of the chip (56) and a plurality of inner leads (53) which surround the chip paddle. The chip paddle and the leads are in a common plane. Conductive wires (58) are used to electrically attach the chip to the leads. A package body is formed by encapsulating with resin (40) the chip paddle, chip, leads and bonding wires, while leaving the lower surface of the leads and the chip paddle exposed. The chip paddle

can be in at least one part thicker than a portion of the leads forming the paddle and leads with an encapsulation-locking feature as taught by Glenn in figures 3-6.

As to **claim 4**, Glenn teaches the chip paddle (figure 8, numeral 24) and a lower surface of the leads (53) are in a common plane. Glenn further teaches features of the chip paddle and the leads in which portions of the chip paddle are thicker than portions of the leads (see figures 3-6).

As to **claim 6**, Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5) that face the chip paddle in the completed package (column 5, lines 31-67, continued to column 6, lines 1 et seq.).

As to **claim 7**, Glenn teaches exposure of the leads at side surfaces (figure 8, numeral 55) and bottom surfaces (32).

As to **independent claim 13**, Glenn teaches a chip paddle (figure 8, numeral 24) which is attached to a chip (56). The chip paddle has an upper surface (25) a lower surface (26) and an intermediate surface (see figure 6). A plurality of leads (figure 8, numeral 53) surround the chip paddle, and the leads and chip paddle form a lead-frame (figure 2). The leads and the chip paddle are in a common plane (figure 8). The chip paddle can be in at least one part thicker than a portion of the leads forming the paddle and leads with an encapsulation-locking feature as taught by Glenn in figures 3-6. The lead-frame is adapted to receive a package body as shown in figure 8, wherein the chip, chip paddle, leads and bonding wires are encapsulated by a resin encapsulant (40). Also, as shown in figure 8, the chip paddle (24) and leads (53) are exposed along the bottom surface.

As to **claim 14**, the applicant recites etching of about 10% to about 90% of the lower side of the paddle. Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5) that face the chip paddle in the completed package (column 5, lines 31-67, continued to column 6, lines 1 et seq.). Further, referring to figures 3 and 4, the surfaces of the leads and chip paddle appear to be almost fully etched. In figure 5, the surfaces of the leads and chip paddle appear to be about half etched (about 50%). For figures 3, 4 and 5, Glenn teaches the etched part to be inside the package body (figure 8 and column 5, lines 31-67, continued to column 6, lines 1 et seq.).

As to **claim 17**, Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5) that face the chip paddle in the completed package (column 5, lines 31-67, continued to column 6, lines 1 et seq.).

As to **claim 18**, Glenn teaches exposure of the leads at side surfaces (figure 8, numeral 55) and bottom surfaces (32).

As to **independent claim 19**, Glenn teaches a lead-frame (figure 2, numeral 20) with a chip paddle (24) which is externally exposed in the package (see figure 8). A plurality of internal leads (53) are disposed around the chip paddle, wherein a lower surface of the leads is also exposed from the package (figure 8). Glenn teaches encapsulation of the lead-frame package, by applying an encapsulant to a surface of the lead-frame which would cover the chip, bonding wires, chip paddle and leads (figure 10, numeral 4). The fluid path, as taught by Glenn, is over the chip, chip paddle and leads so that they are covered by encapsulant. Glenn also teaches features of the

leads and chip paddle which provide a locking feature for encapsulation (see figures 3-6).

As to **claim 20**, Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5) that face the chip paddle in the completed package (column 5, lines 31-67, continued to column 6, lines 1 et seq.).

As to **claim 21**, the applicant recites etching of about 10% to about 90% of the lower side of the paddle. Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5) that face the chip paddle in the completed package (column 5, lines 31-67, continued to column 6, lines 1 et seq.). Further, referring to figures 3 and 4, the surfaces of the leads and chip paddle appear to be almost fully etched. In figure 5, the surfaces of the leads and chip paddle appear to be about half etched (about 50%).

As to **claim 22**, Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5). The etching portion provides a means to lock the encapsulant to the chip paddle and leads (column 4, lines 36 et seq.).

As to **claim 23**, Glenn teaches etching as a means to form the roughened texture of the leads and the chip paddle (figures 3-5). The etching portion provides a reentrant portion for allowing the encapsulant to flow (column 4, lines 36 et seq.).

As to **claim 25**, Glenn teaches an etched portion (figures 3-5) of the chip paddle and leads which is inside the package body when encapsulated (figure 8), an upper surface of the chip paddle and lower surface of the leads in an approximate common plane (figure 8), the chip paddle (figure 8, numeral 24) bonded to a bottom surface of a

chip (56), and a plurality of internal leads (figure 8, numeral 53) with an etched portion (again, see figures 3-5).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn (6,143,981), as applied to claim 1 above, and further in view of Zimmerman (5,172,213).

As noted above, Glenn teaches a lead-frame and chip package. Glenn does not specifically disclose a method of attaching the chip to the chip paddle of the lead-frame. However, Zimmerman teaches a semiconductor chip mounted on a chip paddle with adhesive (column 3, lines 8-19). At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the device of Glenn with an adhesive as taught by Zimmerman such that the chip is permanently bonded to the chip paddle. Even though the chip will be permanently attached to the chip paddle after encapsulation, wherein the encapsulant "marries" the chip paddle to the chip by covering the chip paddle and chip curing to form a hardened structure, it still would be advantageous to use an adhesive. An adhesive would ensure proper placement of the chip to the chip paddle such that the chip would not move from its proper alignment during attaching of bond wires, and flowing of encapsulant material. Further, in view of a manufacturing environment, it would also be advantageous to secure the chip to the chip paddle as the sealing step may be in a different location requiring transferring of

the lead-frame package where the movement could jar the chip out of alignment were it not otherwise securely attached.

Response to Arguments

7. Applicant's arguments filed 9-17-02 have been fully considered but they are not persuasive. As to claim 1, applicant has argued that Glenn et al. does not teach the limitation of the chip paddle being thicker than the leads, with reference to figures 3-6. However, the language of claim 1 (as currently amended) recites: "and wherein the chip paddle is in at least one part thicker than at least a portion of the internal leads". Therefore, Glenn et al. does anticipate the claim, since it is clear from any one of figures 3-6 where a portion of the chip paddle 24 is thicker *than at least a portion* (emphasis added) of the leads 30. Further, none of the claims in the instant application recite where on the leads in relation to where on the chip paddle is one thickness dimension greater or less than another thickness dimension. With this in mind, Glenn et al. does anticipate the thickness limitation of claim 1, and accordingly, claims 4, 13 and 19. As to applicant's arguments under heading #3, 8th paragraph, the examiner did not cite any 35 USC 112 rejections in the previous office action. As to applicant's arguments concerning claim 19, claim 19 has no limitation directed to moisture infiltration caused by short fluid paths. Even assuming that limitation were included in claim 19, Glenn et al. fully anticipates longer fluid paths caused by altering the shape of the ends of the leads and chip paddle, as is seen in figures 3-6, such that the path that could be traveled by moisture from the bottom to top surface is much greater than the actual distance in height from bottom to top surface.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

S.B.G.
November 7, 2002

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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